An Adaptive Bias Controlled Power Amplifier with a Load-Modulated Combining Scheme for High Efficiency and Linearity

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Abstract — This paper presents a highly efficient linear power amplifier with an adaptive bias control circuit. In the amplifier, two amplifiers are power-combined using load modulation networks and then gate biases are controlled according to the input signal envelope. The gate voltage shapes of the two amplifiers have been optimized by envelope simulation to maximize the power added efficiency for the ACLR of −30 dBc. For verification, an adaptively controlled power amplifier has been implemented at 2.14 GHz using 4 watts PEP LDMOSFET's and its bias circuit were constructed based on simulated control shapes. The performances of the amplifier were compared with the class AB and Doherty amplifiers using a one-tone and forward-link WCDMA signals. The measured PAE of the amplifier is 41 % at −30 dBc ACLR, while those of the class AB and Doherty amplifiers are 24.5 % and 28.1 %, respectively.

I. INTRODUCTION

Linearity is the most important figure of merit for the power amplifiers of CDMA base stations. To meet the stringent requirements for linearity, the power amplifiers are usually biased at the class A or AB mode. However, these modes cause a lower efficiency. In addition, due to the high peak-to-average power ratio of CDMA signal, the power amplifiers have to operate with a large amount of back-off of the output power to achieve the linear operation, which further decreases the overall efficiency. As the power capacity of the amplifier increases and the size becomes more compact, the lower efficiency causes a severe thermal problem. Hence, the efficiency of the high power amplifier has become an important issue. The Doherty amplifier is a promising solution for efficiency improvement [1]- [5].

Many research works have tried to realize the Doherty amplifier using a simple bias arrangement for the carrier and peaking amplifiers. In the Doherty amplifier, the peaking amplifier is biased to a class B or C mode, while the bias of the carrier amplifier is set to the class A or AB mode [2]- [5]. The Doherty amplifier with this biasing scheme has the capability to enhance efficiency of the amplifier using a load modulation scheme for asymmetric power combining [1]- [5]. Additionally, the late gain expansion of the class AB peaking amplifier can compensate for the gain compression of the class AB carrier amplifier. Due to the gain expansion and compression characteristics for a properly biased amplifiers, a cancellation of IMD(inter-modulation distortion) terms can be achieved at a

high power level. Actually, we have demonstrated relatively high efficiency with a good linearity in our earlier works [4], [5].

However, though the Doherty amplifier creates higher efficiency and more output power comparable to a class AB amplifier with the same linearity due to the harmonic cancellation, it has some limitations in efficiency improvement. First, the drain current of the peaking amplifier is lower than that of the carrier amplifier because the peaking amplifier is biased at a lower value. Thus, the load impedance of the Doherty amplifier cannot be fully modulated to the value for a high power match. As a result, the carrier and peaking amplifiers cannot generate their respective full powers. The reduced output powers directly limit the improvement of efficiency. Second, because the biases are fixed regardless of power level, undesired dc power consumption arises at a low power level. Third, the harmonic cancellation cannot be optimized according to the power level.

In this paper, we have introduced an adaptive bias control circuit to the Doherty amplifier for further improvement in efficiency. The gate biases of the carrier and peaking amplifiers are controlled according to the envelope of the input signal. Due to the adaptively controlled biases, the output powers generated by the two amplifiers are different according to the power level. Thus, a Wilkinson combiner cannot be used, because it is used to combine the equal output powers. Hence, the load modulation technique of the Doherty amplifier is adopted to combine them, properly, regardless of the ratio of the output powers. The optimum shapes of the gate control voltages are determined using envelope simulation. For verification, the proposed power amplifier is implemented and tested using a one-tone and forward-link WCDMA signals. The amplifier is compared with the comparable class AB and Doherty amplifiers. The test results show superior performances with the proposed amplifier.

II. SIMULATION

Fig. 1 shows the adaptively controlled power amplifier, which consists of a power amplifier with load-modulated combining scheme and an adaptive gate bias control circuits using an envelope tracking technique. The structure of the power amplifier is equal to that of the Doherty amplifier, except the bias control circuit [4], [5]. Due to the adaptive bias circuits, we can improve efficiency as well as linearity by optimizing the gate voltage shapes for both the carrier and peaking amplifiers.
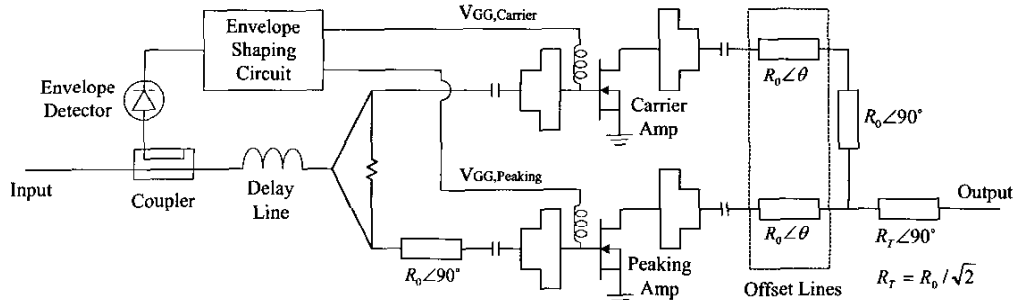
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Fig. 1. Structure of the load-modulated power amplifier with adaptive bias circuit

We have designed the adaptive control circuit with a target of maximizing the power added efficiency (PAE) at –30 dBc ACLR(Adjacent Channel Leakage Ratio). Our target of the –30 dBc has been often used for the base station power amplifiers based on a feed-forward linearization technique [3], [6].
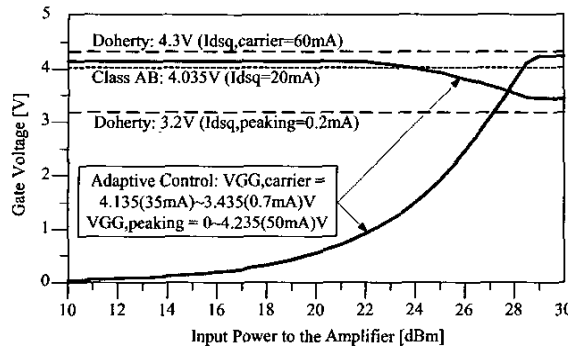

Fig. 2. Simulated optimum bias conditions for class AB, Doherty and adaptively controlled power amplifiers

TABLE I
Simulated performances (at –30 dBc ACLR) under the different bias conditions shown in Fig. 2

Bias Condition	Output Power [dBm]	PAE [%]
Class AB	32.1	25.6
Doherty	32.5	31.0
Adaptive	34.8	45.3

The load-modulated power amplifier has been designed at 2.14 GHz using Agilent's ADS simulator with the model for MRF281SR1 provided by Motorola. The control shapes of gate voltages for both amplifiers according to the envelope of the input signal were generated using a 2-port SDD component. To determine the optimum shapes of gate voltages for both amplifiers, efficiency and linearity were simulated iteratively using envelope simulation. Fig. 2 and Table I show the generated optimum shapes and the simulated average output power and PAE (with –30 dBc ACLR), respectively. The simulated results were compared with the class AB and Doherty biased amplifiers as their counterparts. Notice that the carrier amplifier of the

Doherty amplifier was biased more highly than the class AB amplifier in this work. This bias scheme creates a linearization due to the cancellation of IMD3 generated by the carrier and peaking amplifiers [4], [5]. The simulated results show that the adaptively controlled power amplifier is superior by far to the Doherty amplifier, as well as the class AB. The adaptively controlled power amplifier has 45.3 % of PAE, which is about 14 % higher than that of the Doherty amplifier.

III. IMPLEMENTATION

The 2.14 GHz load-modulated power amplifier has been implemented using Motorola's MRF281SR1 (4 watts PEP) LDMOSFET's. The amplifier has been power-matched to $R_0 = 50 \Omega$ so that its source and load matching impedances are $Z_S = 3.1-j3.5 \Omega$ and $Z_L = 11.36+j7.94 \Omega$, respectively. The design process including the offset lines was presented in our earlier works [4], [5]. In this experiment, the 0.535 λ lengths of offset lines were used for both the carrier and peaking amplifiers. The output impedance transformed by the line becomes 344 Ω, which is high enough to block the output power leakage to the peaking amplifier at a low power operation. Fig. 3 shows a photograph of the implemented amplifier.

To adopt the simulated optimum shapes to a real circuit, we constructed an adaptive gate bias circuit, as shown in Fig. 4. It contains the envelope detector and envelope shaping circuits. A 10 dB directional coupler, a 6 dB attenuator, a Shottky detection diode, and a low pass filter have been used to obtain the appropriate envelope signal level. For the envelope shaping circuit, we have constructed two separated paths to generate independently the control voltage of the carrier and peaking amplifiers. The upper path is for the carrier amplifier, which consists of two stages; a inverting voltage amplifier stage and a dc offset voltage adder stage. The lower path is for the peaking amplifier, which consists of two non-inverting voltage amplifiers. The respective stages for the upper and lower paths have an AD829 OP Amp with 600 MHz gain bandwidth product and additional passive components. We have experimentally optimized the values of the components to achieve the maximum PAE with –30 dBc ACLR at 2.5 MHz offset for a forward-link WCDMA signal, which has a chip rate of 3.84 Mcps and a peak-to-average ratio of 8.6 dB at 0.1 % CCDF. The optimized values of the components, also, are shown in Fig. 4. Finally, a coaxial

line has been used for the delay line, but it can be replaced by a delay filter with low loss and low cost.
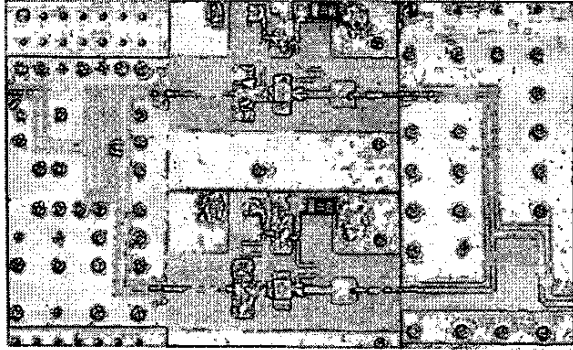

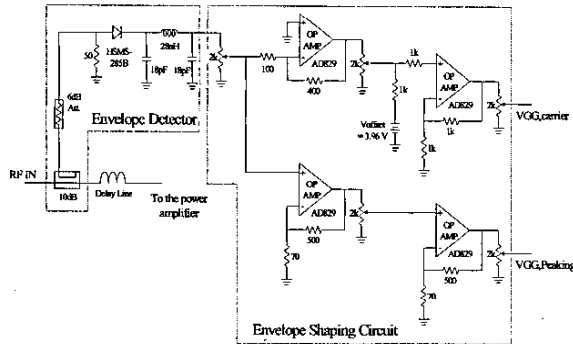Fig.3. Photograph of the load-modulated power amplifier

Fig. 4. Circuit diagram for the adaptive gate bias circuit

IV. EXPERIMENTS

We compared the performances of the adaptively controlled power amplifier with those of the class AB and the conventional Doherty amplifier using one-tone and forward-link WCDMA signals. The class AB amplifier can be achieved by simply class AB biasing both the carrier and peaking amplifiers. In these experiments, quiescent currents for both the carrier and peaking amplifiers were set to 20 mA for the class AB amplifier. In the case of the conventional Doherty amplifier, on the other hand, quiescent currents of the carrier and peaking amplifiers were set to 60 mA and 0.1 mA, respectively. These current levels are experimentally optimized to enhance linearity to near −30 dBc ACLR. The gate voltages of the adaptively controlled power amplifier have been controlled by the shapes shown in Fig. 5, which have been generated by the circuit shown in Fig. 4. The experimentally optimized bias conditions for the respective amplifiers are similar to the simulated one.

Fig. 6 shows the measured PAE's versus output power of the class AB, Doherty and adaptively controlled power amplifiers, when a 2.14 GHz CW signal is applied. The PAE of the adaptively controlled power amplifier was improved significantly throughout a wide power range compared to the

class AB and Doherty amplifiers. This enhanced performance is due to reduction of unnecessary dc power consumption of the peaking amplifier and appropriate bias shaping according to power level.
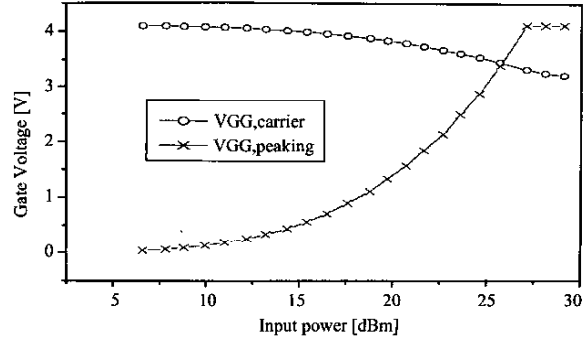

Fig. 5. Control shapes of gate voltage for the adaptively controlled power amplifier
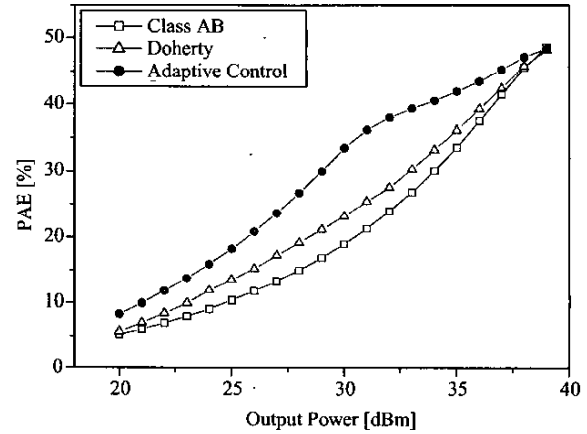

Fig. 6. Measured PAE's of the class AB, Doherty and adaptively controlled power amplifiers, when a CW signal is applied

The test results for a forward-link WCDMA signal have been represented in Fig. 7. Fig. 7(a) shows that the adaptively controlled power amplifier has a significantly improved average PAE relative to the class AB and Doherty amplifiers due to the enhanced efficiency throughout the wide envelope power range, as shown in Fig.6. Fig. 7(b) shows the measured ACLR's at 2.5 MHz offset. The adaptively controlled power amplifier has clearly a better linearity at a high output power level due to the appropriate biases shaping of the carrier and peaking amplifiers. At a low power level, however, the linearity for harmonic cancellation is degraded. This degradation of ACLR at the low power level is not a problem because our target has been focused on ACLR level of −30 dBc for all output power level and optimized for it. We have summarized numerically the test results for a forward-link WCDMA signal in Table II. At an −30 dBc ACLR, the average PAE of the adaptively controlled power

amplifier has been improved to 41 %, which represents a 16.5 % and 12.9 % improvements compared to the class AB and Doherty amplifiers, respectively. It has also produced 2.2 dB and 1.4 dB more output power, respectively.
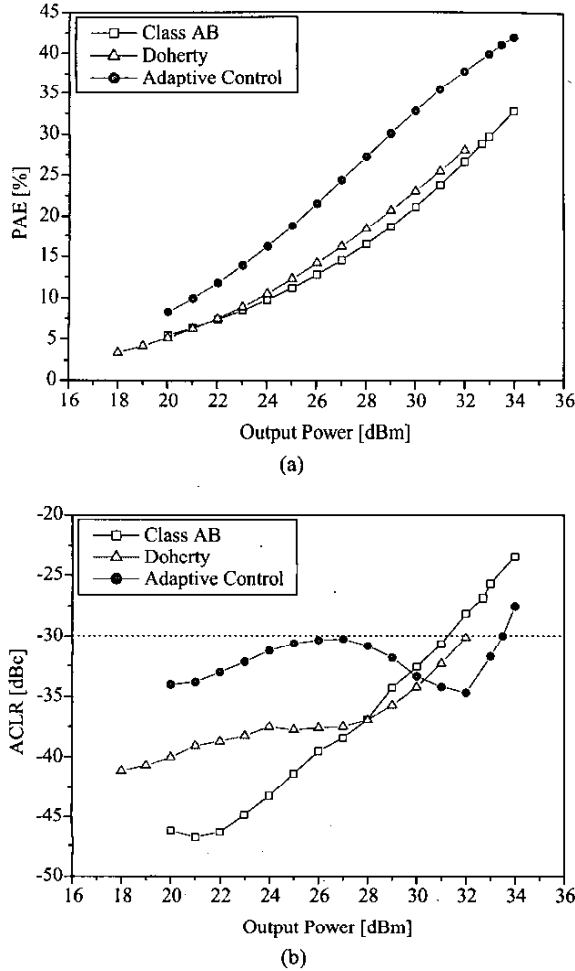

(a)

(b)

Fig. 7. Measured (a) PAE's and (b) ACLR's of the class AB, Doherty and adaptively controlled power amplifiers, when a forward-link WCDMA signal is applied

TABLE II
Measured performances with –30 dBc ACLR for a WCDMA signal under the different bias conditions

Bias Condition	Output Power [dBm]	PAE [%]
Class AB	31.3	24.5
Doherty	32.1	28.1
Adaptive	33.5	41.0

V. CONCLUSIONS

For base station application, a highly efficient linear power amplifier with an adaptive bias circuit has been proposed. The gate biases of the carrier and peaking amplifiers are controlled according to the input signal envelope. In order to properly combine the asymmetric output powers of the amplifiers, the amplifier contains a load-modulated combining network. The most important advantage of the amplifier relative to the conventional Doherty amplifier is that the gate voltages can be freely controlled to enhance efficiency and linearity. It has been supported by the simulated results. For experimental verification, a 2.14 GHz adaptively controlled power amplifier has been implemented using Motorola's MRF281SR1 (4 watts PEP) LDMOSFET's and tested using a one-tone and forward-link WCDMA signals. For a forward-link WCDMA signal, the proposed power amplifier has PAE of 41 % with 33.5 dBm average output power at –30 dBc ACLR, which is an improvement of 16.65 % and 12.9 % in efficiency and 2.2 dB and 1.4 dB in output power relative to the class AB and Doherty amplifiers at the same ACLR level. These experimental results clearly demonstrate that the adaptively controlled power amplifier is the best performing amplifier for the base station power application that requires high efficiency as well as good linearity.

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